Remarks:

Reconsideration of the application is requested.

Claims 1-20 are now in the application. Claims 1-20 are subject to examination and claims 21-25, which were previously withdrawn from examination, have been canceled. Claim 1 has been amended. No new matter is believed to have been added.

In regard to the Examiner's statements in the second paragraph under "Election/Restrictions" on page 2 of the above-identified Office Action, non-elected claims 21-25 have been canceled. Applicants reserve the right to reintroduce such claims at a later date.

In the first paragraph under "Claim Rejections - 35 U.S.C. § 112" on page 2 of the above-identified Office Action, claims 1-21 have been rejected as being indefinite under 35 U.S.C. § 112, second paragraph.

It is assumed that the Examiner intended to reject only claims 1-20 and did not intend to include claim 21 in the rejection, because claim 21 is non-elected.

More specifically, the Examiner again states that the use of the term "spacer layer" in claim 1 is inconsistent with the

usual meaning of that term. The Examiner states that the term is used "in claim 1 to mean 'separation/filler' while the accepted meaning (of "spacer layer") is a 'sidewall spacer.' The Examiner suggests using "separation" instead of "spacer" and further states that "a spacer layer is generally understood to mean a layer on the sidewalls of a gate and a separation layer is generally understood to mean a layer that separates two other elements."

Applicants respectfully disagree with the Examiner's statements and submit that they are not using the term (spacer layer) inconsistent with its normal meaning. The specific meaning of that term has not been memorialized necessarily to have the definition as stated by the Examiner. Applicants have chosen to use the term to define the layers 3 and 5 as disclosed in the instant application, which is not inconsistent with the normal and usual meaning of that term. For example, on page 12, lines 9-11 the spacer layer 5 is described as "spacer material for a gate electrode that is to be used in its place." Also, Webster's Dictionary defines "spacer" to mean "a device or piece for holding two members at a given distance from each other." The references of Chan (col. 4, lines 37-38), Hu (col. 4. lines 10-12), Miyamoto (see col. 8, lines 5-6, where channels 6,6a are "separated" from gates 8,8a by oxide film 7), and Gambino (col. 3, lines 31-33) disclose different uses and meanings of the term "spacer,"

respectively. The term is not necessarily limited to the Examiner interpretation "of a layer on the sidewalls of a gate." Applicants have used the term "spacer" throughout the instant specification and in the claims of the instant application in a manner that is believed to be clear and understood by one skilled in the art to which the present invention pertains. Contrary to the Examiner's statement, the term "spacer" is used in a manner which is not repugnant to the usual meaning of that term. Therefore, the use of the term "spacer' has been retained in the instant claims.

It is accordingly believed that the claims meet the requirements of 35 U.S.C. § 112, second paragraph. The above remarks are provided solely for the purpose of explaining the present invention. They are neither provided for overcoming the prior art nor do they narrow the scope of the claim for any reason related to the statutory requirements for a patent.

In the last paragraph on page 3 of the Office action, claims 1-2 and 4-20 have been rejected as being obvious over Chang et al. (U.S. Pat. No. 6,365,465), presumably the Examiner intended to refer to Chan et al. because the '465 patent is in the name of Chan et al., (hereinafter "Chan") in view of Burghartz et al. (U.S. Patent No. 5,461,250) (hereinafter "Burghartz") under 35 U.S.C. § 103(a).

The rejection has been noted and the claim 1 has been amended in an effort to even more clearly define the invention of the instant application. Support for the changes is found on pages 3-4 and in the corresponding descriptions of each of the steps of the present invention in the instant specification.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 calls for, inter alia, a method for fabricating a double gate MOSFET, which comprises the steps **in the following sequence**:

providing a substrate structure having a silicon substrate layer;

patterning the semiconductor layer resulting in a semiconductor layer structure provided as a channel of the double gate MOSFET;

depositing a second spacer layer on the semiconductor layer structure and the first spacer layer;

completely embedding the semiconductor layer structure in the first and second spacer layers by patterning the first and second spacer layers;

depositing a second insulation layer on a structure formed of the first and second spacer layers;

vertically etching two depressions disposed along one direction, the two depressions dimensioned such that the semiconductor layer structure is situated completely between them, during the etching of the two depressions, the second insulation layer, the first and second spacer layers and, in each case on both sides, an edge section of the semiconductor layer structure being etched through completely in each case;

filling the depressions with an electrically conductive material;

forming a contact hole in the second insulation layer;

selectively removing the first and second spacer layers through the contact hole made in the second insulation layer;

applying third insulation layers on inner walls of a region of removed spacer layers and on surfaces of the semiconductor layer structure; **and**

introducing a further electrically conductive material into the region of the removed spacer layers.

Accordingly, the present invention is directed to a method for fabricating a double gate MOSFET transistor in a particular sequence. A semiconductor layer structure of a transistor channel is fully embedded in a spacer material, and is contact-connected by source and drain regions (which are filled into depressions that are etched on opposite sides of the semiconductor layer structure). Next, the spacer material is etched out selectively, and is replaced by the electrically conductive gate electrode material.

The Chan reference discloses a method for forming a double-gate MOSFET transistor. The method utilizes a selective lateral epitaxial growth of silicon from an existing single crystal silicon MOSFET channel to form the source/drain regions. The source/drain regions are bounded by pre-defined dielectric boundaries and are thereby limited in size to the local source/drain regions.

The dielectric which bounds the selective epitaxial growth is used as a self-aligned implant mask for selectively forming the heavily doped source/drain regions. The dielectric is removed after the source/drain formation to form a suspended silicon channel. The gate insulator and the gate electrodes are subsequently formed to complete the MOSFET.

Accordingly, applicant points out that there are differences between the fabrication method of the present invention and that of Chan. The manner of forming the structure of Chan is totally different from the claimed method. In the present invention, the first and second spacer layers are patterned such that the semiconductor layer structure **remains completely embedded in the first and second spacer layers.** In contrast to Chan, the present invention discloses that the channel forming layer 4A is completely embedded by the layers 3 and 5. See Fig. 4 of the instant application. The Examiner acknowledges that Chan is deficient is this respect and attempts to make up for the deficiency with the disclosure of Burghartz. Additionally, claim 1 recites that the steps according to the present invention are **performed in the recited sequence,** which enables obtaining the advantages and benefits of the present invention, namely, an accurate alignment of the topside and underside gates in a technologically uncomplicated and relatively simple manner. Thus, for example, after the recited step of "patterning the semiconductor layer resulting in a semiconductor layer provided as a channel of the double gate MOSFET", the next step that follows is a step of "depositing a second spacer layer on the semiconductor layer structure and the first spacer layer." This is not true of Chan in which there is no depositing step of a second spacer layer after the patterning

step (shown in Fig. 2g of Chan), as recited in claim 1 of the instant application.

Neither does Burghartz overcome the deficiencies of Chan. Nor is Burghartz properly combinable with Chan.

It is submitted that the Examiner has not shown and articulated sufficient teaching, motivation, or suggestion in the prior art for combining Chan and Burghartz.

The reference numerals corresponding to the above-features are presented solely for illustrative purposes. They are not intended to narrow the scope of the claims for any reason whatsoever.

Clearly, the references do not show or teach "a method for fabricating a double gate MOSFET, which comprises the steps **in the following sequence: providing a substrate** structure having a silicon substrate layer; **patterning** the semiconductor layer resulting in a semiconductor layer structure provided as a channel of the double gate MOSFET; **depositing a second spacer layer** on the semiconductor layer structure and the first spacer layer; **completely embedding the semiconductor layer structure in the first and second spacer layers by patterning the first and second spacer layers; depositing a second insulation layer** on a structure formed of the first and second

spacer layers; **vertically etching two depressions** disposed along one direction, the two depressions dimensioned such that the semiconductor layer structure is situated completely between them, during the etching of the two depressions, the second insulation layer, the first and second spacer layers and, in each case on both sides, an edge section of the semiconductor layer structure being etched through completely in each case; **filling the depressions** with an electrically conductive material; **forming a contact hole** in the second insulation layer; **selectively removing** the first and second spacer layers through the contact hole made in the second insulation layer; **applying third insulation layers** on inner walls of a region of removed spacer layers and on surfaces of the semiconductor layer structure; **and introducing a further electrically conductive material** into the region of the removed spacer layers", as recited in claim 1 of the instant application.

In the second paragraph on page 8 of the Office Action, claim 3 has been rejected as being obvious over Chan in view of Shimizu (U.S. Pat. No. 5,753,541) under 35 U.S.C. § 103(a).

The foregoing discussion of Chan is equally applicable in the rejection of claim 3, which depends from claim 1.

Shimizu does not overcome the deficiencies of Chan (and Burghartz, even if the Examiner relied in the latter reference, which he has not, as an additional secondary reference in the rejection of claim 3).

A critical step in analyzing the patentability of claims pursuant to 35 U.S.C. § 103 is casting the mind back to the time of invention, to consider the thinking of one of ordinary skill in the art, guided only by the prior art references and the then-accepted wisdom in the field. See In re Dembiczak, 175 F.3d 994, 999, 50 USPQ2d 1614,1617 (Fed. Cir. 1999). Close adherence to this methodology is especially important in cases where the very ease with which the invention can be understood may prompt one "to fall victim to the insidious effect of a hindsight syndrome wherein that which only the invention taught is used against its teacher." Id. (quoting W.L. Gore & Assocs., Inc. v. Garlock, Inc., 721 F.2d 1540, 1553, 220 USPQ 303, 313 (Fed. Cir. 1983)).

Most if not all inventions arise from a combination of old elements. See In re Rouffet, 149 F.3d 1350, 1357, 47 USPQ2d 1453,1457 (Fed. Cir. 1998). Thus, every element of a claimed invention may often be found in the prior art. See id. However, identification in the prior art of each individual part claimed is insufficient to defeat patentability of the whole claimed invention. See id. Rather, to establish

obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the specific combination that was made by the appellant. See In re Dance, 160 F.3d 1339, 1343, 48 USPQ2d 163.5, 1637 (Fed. Cir. 1998); In re Gordon, 733 F.2d 900, 902, 221 USPQ 1125,1127 (Fed. Cir. 1984).

The motivation, suggestion or teaching may come explicitly from statements in the prior art, the knowledge of one of ordinary skill in the art, or, in some cases the nature of the problem to be solved. See Dembiczak, 175 F.3d at 999, 50 USPQ2d at 1617. In addition, the teaching, motivation or suggestion may be implicit from the prior art as a whole, rather than expressly stated in the references. See WMS Gaming, Inc. v. International Game Tech., 184 F.3d 1339, 1355, 51 USPQ2d 1385, 1397 (Fed. Cir. 1999). The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art. See In re Keller, 642 F.2d 413, 425, 208 USPQ 871, 881 (CCPA 1981) (and cases cited therein). Whether the examiner relies on an express or an implicit showing, the Examiner must provide particular findings related thereto. See Dembiczak, 175 F.3d at 999, 50 USPQ2d at 1617. Broad conclusory statements standing alone are not "evidence."

Id. When an Examiner relies on general knowledge to negate patentability, that knowledge must be articulated and placed on the record. See In re Lee, 277 F-3d 1338, 1342-45, 61 USPQ2d 1430, 1433-35 (Fed. Cir. 2002).

Upon evaluation of the Examiner's comments, it is respectfully believed that the evidence adduced by the Examiner is insufficient to establish a prima facie case of obviousness with respect to the claims. Accordingly, the Examiner is requested to withdraw the rejection.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art. The dependent claims 2-20 are believed to be patentable as well because they all are ultimately dependent on claim 1.

In view of the foregoing, reconsideration and allowance of claims 1-20 are solicited.

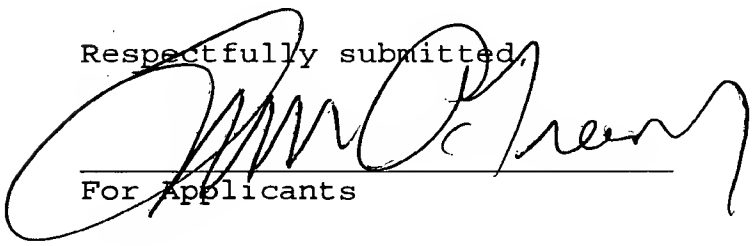
In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out. In the alternative, the entry of the amendment is requested, as it is believed to place the application in

better condition for appeal, without requiring extension of the field of search.

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,



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